Hysteresis Correction and its Relationship to Creep and Drift in Scanning Tunneling Microscope Tip Positioning

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Phosphorus in silicon qubits in geometries as defined by Scanning Tunneling Microscope (STM) lithography is a promising architecture, at least for a few qubits. However, as the number of qubits increases to occupy a surface area of 1μm^2 or greater, positioning errors which increase nonlinearly with step lateral step size will become difficult to correct for multi-level systems. While methods for correcting positions are available such as lattice registration, artificial fiducial registration, and closed loop positioning, this model-based compensation for position uncertainties greatly reduces patterning time for highly scaled devices.

This work shows that the hysteresis error for the commonly used ScientaOmicron VT STM to be approximately $0.03r^2$ μm where r is the size of a lateral step. Furthermore, it is shown that creep corrections described previously depend upon the state of the hysteresis with observed creep coefficients varying by over 10%. A real-time correction algorithm with 20-bit precision and 50 μs update time will be described. This algorithms reduces positioning errors for 2μm steps from >100nm down to <20nm. Furthermore, correcting hysteresis reduces the variability of optimal creep correction coefficients. Results will be shown for lateral motion as well as settling times in Z as shown below, with the effects of position correction on complex patterns shown.

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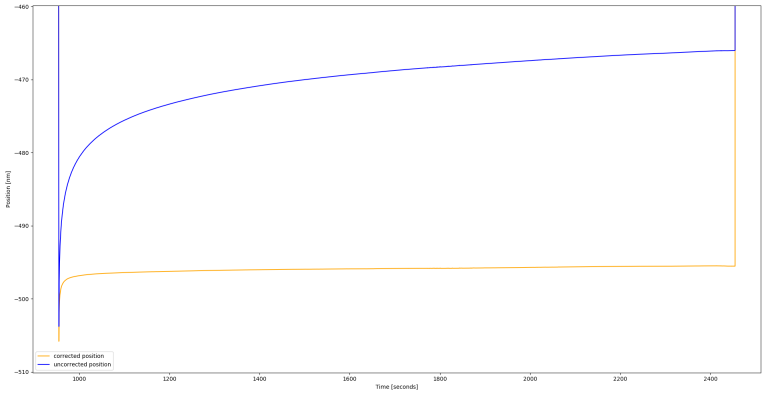

Figure 1: Comparison of Z settling after 1 μm retraction with and without creep and hysteresis correction. The expected position is -500 nm.