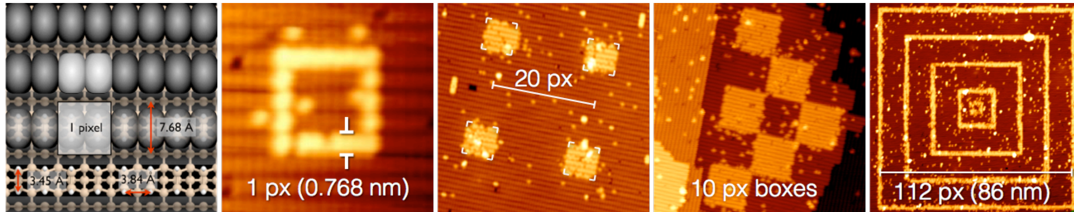
Automated STM lithography for P-in-Si multi-qubit devices

J. H. G. Owen, J. Ballard, E. Fuchs, J. N. Randall and J. R. Von Ehr

Zyvex Labs LLC, 1301 N. Plano Rd, Richardson, TX 75081, USA.

E-mail: jowen@zyvexlabs.com



Atomic-scale P-in-Si devices have been created using H depassivation lithography (HDL) to create patterns on Si(001), which are filled with P atoms, forming the 'single-atom transistor' and 1.5 nm wide wires with Ohmic conductivity [1,2]. The precise atomic-scale distances between the different elements of these devices have a strong effect on their properties. Thus, in order to scale up to future multi-qubit devices where yield and reproducibility of their properties become critical, the accuracy and precision of the fabrication technology needs to be improved.

We have developed a control system to perform automated HDL patterning. We have defined a pixel size of two dimers on one dimer row on the Si(001) surface, which is a 7.68 Å square. The tip moves directly to the area to be patterned, and writes along vectors whose directions are defined by the surface atomic lattice. Sources of error such as thermal drift and piezo creep are corrected in real time to maintain atomic precision in the tip position. As a result, within an area of about 100 nm, we can draw arbitrary patterns with an error of at most 1 px. Furthermore, the whole process can be automated, thus greatly improving reproducibility of the final device pattern.

A critical pattern to be drawn for P-in-Si qubit devices is the 3-dimer pattern, which is required for placement of a single P atom, as in the 'single-atom transistor'. For such small features, i.e. lines just a few pixels long, end effects and tip variability become significant. We have test scripts which begin and end the write vector at different locations within the patterning pixel, either on top or between the Si dimers, so as to explore the effect on the overall line length. In this way, we can calibrate the optimal subpixel start and end points for each tip before beginning a pattern, so as to maximise the yield of the desired length for arbitrary atomic-scale patterns, and thus the yield of the overall devices.

1. Weber *et al*. Science **335**, 64-67 (2012).
2. Fuechsle *et al.* Nature Nanotechnology **7**, 242-246 (2012).