# Automated Atomically Precise Lithography over Multiple Length Scales for Complete Nanodevice Fabrication

J. H. G. Owen*, J. Ballard, S. Schmucker, E. Fuchs, J. N. Randall and J. R. Von Ehr
*Zyvex Labs LLC, 1301 N. Plano Rd, Richardson, TX 75081, USA.*
*jowen@zyvexlabs.com*

Various atomic-scale P-in-Si electronic devices such as the 'single atom transistor'[1] have been fabricated with near-atomic precision using a Scanning Tunnelling Microscope (STM) tip to perform H depassivation lithography (HDL), writing patterns on a Si(001) surface, into which $PH_3$ is adsorbed, which is then incorporated into the silicon surface and buried by Si overgrowth. As shown in the figure, the patterning of such devices requires precise positioning across several length scales, from the 3-dimer pattern for the single P atom, the ~10 nm gaps of the immediate electrodes, such as source and drain, and control gates, up to the ~1 µm scale of the bond pads, which connect the device to the outside world. We have developed an automated STM lithography system, which can write all parts of such devices with the required precision, so that complete nanoscale devices can be written from a pattern input file without operator intervention. For the atomic details of the device, the tip is aligned to the Si lattice, writing to a pixel grid, where 1 pixel(px) comprises 4 Si atoms (0.768 nm sq) and patterns are written using tip vectors moving along or across the Si(001) dimer rows. We have developed a process for real-time correction of piezo creep. In our position precision testing, errors can be reduced to less than 1 px over areas of around 100 nm, and with errors of around 1% over 500 nm areas. For larger length scales, where hysteresis errors become a significant issue, our software can automatically re-align the tip position when necessary to prewritten fiducial marks, so that errors do not accumulate. By these means, we can greatly increase the yield and reproducibility of STM lithography, and automate the writing of complex atomic-scale patterns.

1: M. Fuechsle, J. A. Miwa, S. Mahapatra, H. Ryu, S. Lee, O. Warschkow, L. C. L. Hollenberg, G. Klimeck, and M. Y. Simmons *Nat Nano* **7** 242-246 (2012)

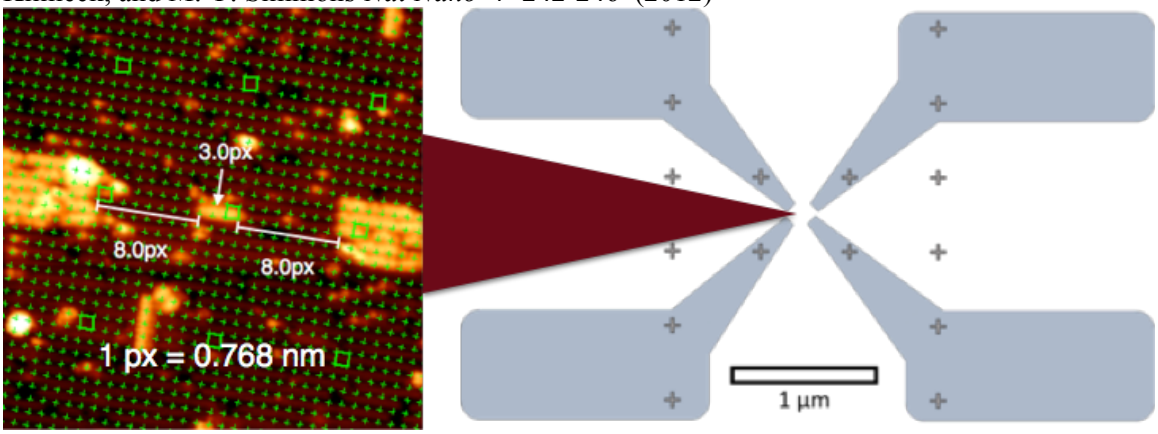


Figure 1. Left: An atomic-scale device. 1 px = 4 atoms = 0.768 nm. A 3px line is drawn to enable incorporation of a single P atom. Source and drain electrodes are drawn exactly 8 px (6 nm) away from the 3-px pattern. Right: The central device region is surrounded by µm-scale bond pads.