Advances in Precision for Digital STM Lithography on Silicon

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Hydrogen depassivation lithography has enabled unprecedented sub-nanometer precision in the positioning of dopant atoms in silicon,[1] advancing the field of silicon quantum electronics. However, as donor-based QIP devices scale from single-qubit devices towards multi-qubit devices such as crossbar architectures[2], atomically precise lithography is required over increasingly large areas with improved reproducibility.

After developing the ZyVector™ automated STM lithography system with real-time piezo creep correction, we have previously demonstrated open-loop atomic precision patterning (i.e. lithography errors of less than one dimer row or pixel (Fig.1a)) over length scales up to 100 nm [Fig. (1b)]. On scales up to 500 nm, the position errors were up to 2.5%, with hysteresis errors becoming more significant over larger areas.

In this work, we address these errors while continuing to optimize the correction of piezo creep, and also correction of hysteresis. Comparisons between patterns written with and without real time positioning corrections will be offered [Fig (1c,d)]. For movements within small areas, creep correction reduces positioning errors by more than 90%. Hysteresis corrections for further reducing open-loop position errors will be described. A method of closed-loop navigation further reduces positioning error; the pattern can be divided into write fields, within which precise patterning can be achieved. Write fields are then stitched through the use of deliberately written fiducial marks or recognition of previously written patterns. Thus, the precise patterning can be scaled over large areas.

Taking all these techniques together, we present a set of design rules, which will allow for successful patterning from the single-atom to the micron scale, allowing fabrication of the next generation of dopant-based QIP devices.

1 M. Fuechsle, et al. *Nat Nano* **7** 242-246 (2012)
2 C. D. Hill, et al. *Science Advances* **1** (2015)

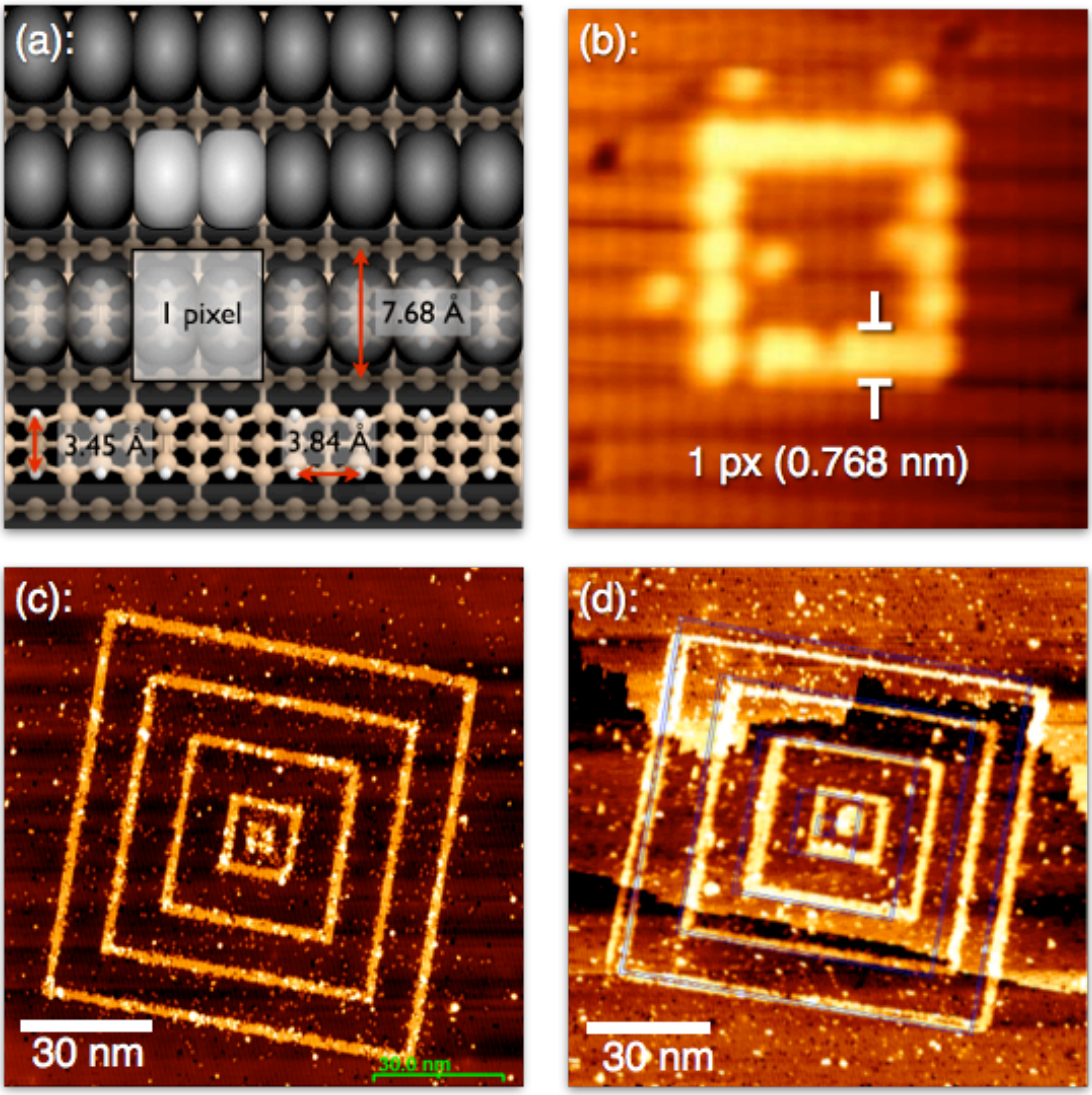

Figure 1: (a): We have defined a lithography pixel as a pair of Si dimers on a single dimer, giving a square pixel 7.68 Å wide. (b): STM lithography of a box, with a linewidth of 1 px. (c,d): A test pattern comprising 5 pairs of 1-px rectangles, largest is 112 px (86 nmwide), drawn with and without creep correction applied, respectively.