Patterned atomic layer epitaxy of Si/Si(001):H

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We aim to develop techniques for the building of atomically precise structures. On the H-terminated Si(001) surface, H atoms can be selectively removed using an STM tip with appropriate lithography conditions, creating arbitrary patterns of reactive dangling bonds with atomic precision. The exposed patterns are used as templates for the growth of Si and Ge by gas-source epitaxy, using disilane and digermane as the precursor gases. The quality of the epitaxy, in terms of island size and defect density of the second and subsequent monolayer (ML), is dependent upon the electron exposure. Good-quality growth of the second and following MLs requires a multiple of the exposure required for good-quality growth of the first ML. This is interpreted in terms of remanent hydrogen in island sites in the first ML. © *2011 American Vacuum Society*. [DOI: 10.1116/1.3628673]

I. INTRODUCTION

We aim to develop techniques for atomically precise manufacturing (APM), that is the fabrication of structures with the ultimate available precision — one atom. Our current efforts in this direction are directed towards the growth of silicon and germanium structures on the Si(001) surface, using H termination as a mask, and scanning Tunneling microscope (STM) depassivation as the lithographic process. With appropriate lithographic conditions, it is possible to remove single H atoms[1,2] and to write lines of dangling bonds 1–2 atoms wide. The removal of the H atoms exposes Si dangling bonds in arbitrary patterns, which are highly reactive. In previous work, such dangling bond lines have been used for metal deposition, to form atomic-scale wires.[3] However, the deposited metal will often form disordered clusters rather than epitaxial wires.[4] Deposition of Si or Ge onto the exposed patterns is expected to grow epitaxially, to form well-ordered crystalline structures. However, single atoms evaporated from solid sources are reactive with the H passivation layer[5,6] and thus the monohydride surface will not act as a growth mask in this case. To achieve localized deposition, we therefore use disilane and digermane as precursors, which are unreactive with the monohydride surface. The reaction of these gases with the Si(001) surface has been well-studied previously, by a variety of techniques. Scanning tunneling microscopy data[7–10] has found that the disilane breaks down upon adsorption, forming short islands of addimers which broaden into rectangular epitaxial islands at higher temperatures. The aspect ratio of these islands is much less than that found at a similar temperature range with solid–source deposition.[11] This effect has been put down to the presence of surface H, which with even a 4% coverage, effectively doubles the activation barrier of Si diffusion.[12] Patterned Epitaxy of Si or Ge on Si(001) falls in between solid-source MBE growth and gas-source chemical vapor deposition(CVD), as at the growth temperatures used, 550–600 K, the reaction self-terminates due to saturation of all available dangling bonds by disilane fragments or H atoms resulting from the dissociation of the disilane. This H must then be removed by STM lithography, so that further Si can be deposited. In this work, we discuss the effect of this H on the ability to grow multiple-layer structures of Si by Patterned Epitaxy, and discuss the methods for achieving the optimal growth quality.

II. DESCRIPTION OF METHODS

A. STM lithography

Scanning tunneling microscope lithography is effectively a form of variable spot size electron beam lithography, and is discussed in more detail elsewhere.[13] At low biases, multiple electrons are pumped into a Si-H bond, exciting the bonding electrons up the vibrational energy levels until the bond breaks. Above about 7 V, a single electron has enough energy to break the bond by itself, and a higher-yield process becomes operational.[14] For large-scale patterning, the high-V process has the advantage of a wider linewidth, and a much greater yield per electron. For atomically precise structures; however, the linewidth and the significant edge roughness become a liability, and the low-voltage process, which can in principle be used to remove single H atoms from a surface, becomes favored. For the APM applications that are our ultimate goal, a hybrid process, using the low-V lithography for the edges, and the high- V lithography to fill in the larger areas, is likely to be necessary. Lithography tests for a variety of voltage, current and electron dose parameters are used to search for optimal parameters. Typical electron doses required to remove more than 90% of the H atoms along a line are about 0.1 mC/cm for high-V lithography and 4 mC/cm for low-V lithography. In this work, patterns are written by moving the STM tip along a series of horizontal lines, to draw a square box 20×20 nm at a constant speed. Performing lithography with atomic precision imposes stringent

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stability requirements, and all lithography is performed at growth temperature, as the drift consequences of changing the temperature would make the repeated cycling necessary for multilayer growth unfeasible. The maximum temperature for performing lithography is about 600 K, as above this temperature, the hydrogen making up the pattern becomes mobile.[15] Moreover, for the case of Ge growth, digermane attacks the background passivated layer, forming unwanted dimer islands in this temperature range.

B. Patterned epitaxy

Patterned Epitaxy proceeds by a series of steps, which are illustrated in Fig. 1(a). First, the Si(001) surface must be stabilized at growth temperature, which typically takes 2–3 hs to achieve a drift level of a few nm/hour. Due to the severe drift issues associated with changes in temperature, it is necessary to maintain the sample at the growth temperature at all times. The pattern is written in the H-terminated Si(001) surface using an STM tip, as shown schematically as Step 2 in Fig. 1(a). Typical writing parameters are 8 V, 2 nA, and an electron exposure of 0.1 mC/cm, which is found in experiment to give a linewidth of about 5 nm. The tip is then retracted about 100 nm, to reduce tip shadowing of the sample, and a pulse of disilane is introduced into the UHV through a doser directed towards the sample, Step 3 in Fig. 1(a). The pulse is quantified from the peak background pressure, which is in the range of $1–3 \times 10^{-6}$ Torr for 10 s. Modeling of the gas doser suggests that the actual flux impinging on the sample surface is a factor of 10 greater than this, corresponding to a dose of 100 L. After the dose, the tip is reapproached, and the disilane-saturated pattern is reacquired. There is some drift or piezo creep associated with the tip retraction, so it is necessary to scan 1–2 images to stabilize, before the lithography step can proceed. After adsorption at 550–600 K, the saturated pattern typically shows a mixture of small islands of a few dimers, ad-dimers, and smaller features, which are assumed to be unreacted fragments of disilane. STM lithography is then performed on the disilane-saturated pattern to strip the H off the disilane fragments, Step 4 in Fig. 1(a). During this process, there is significant rearrangement of the disilane fragments, and short islands are formed. The typical amount of Si deposited in one cycle is 1/3–1/4 ML Si. Then the disilane dose is repeated, Step 5 in Fig. 1(a). By cycling between doses of disilane and STM lithography, multiple cycles of Si can be deposited, gradually building up many ML of Si, Step *n* in Fig. 1(a).

An example of the Patterned Epitaxy is shown in Fig. 1(b). In this example, three cycles of digermane deposition have been used to grow about 1 ML of Ge. The nominal pattern size is 20×20 nm, and a minimal exposure of electrons has been used, 0.1 mC/cm at 9 V, 3 nA. The majority of island nucleation takes place in the first cycle and the subsequent cycles cause these islands to grow and merge. Using these conditions, the typical island nucleate as single dimer strings 5–10 dimers long, although some wider islands are already visible after the first cycle of deposition and H removal. After three cycles, the islands have grown and merged, although some gaps remain between islands, which are likely to be antiphase boundaries between the dimerization of the two neighboring islands.[16,17] Even before the complete filling in of the first layer, the second layer islands have nucleated. Note that the aspect ratio of these islands is very short, much more in common with those from gas-phase Si epitaxy,[17] than the long, narrow islands found with MBE growth from solid sources.[16]

III. RESULTS

At the temperature used here, conventional MBE can grow epitaxially for many layers. However, in our case, we observe roughness to increase from layer to layer, even in the second monolayer. The difference here is likely to be some hydrogen which is not removed by the lithography process, and remains on the surface. The presence of even a small amount of surface H is known to affect strongly the morphology of the growth[11] in this temperature range, effectively doubling the Si diffusion barrier. In particular, the primary surface sites for island growth, such as the dangling bonds at the ends of dimer islands, are also preferential adsorption sites for H. Moreover, while adsorption of Si atoms in the antiphase boundaries between islands is a high-energy situation, the adsorption of SiH_2 groups in these locations is likely to be preferred, and would adversely affect the possibility of fill-in and overgrowth. To test the effect of removing the last few percent of surface H, we have conducted growth experiments in which four different electron doses are used within the same large area, and then the morphology of the resulting Si can be directly compared, as other variables such as substrate temperature and precise disilane flux are constant. Images taken after the first lithography step, after three cycles ($\sim$1 ML), and after six cycles ($\sim$2 ML), are shown in Fig. 2(a). The conditions for the top-left pattern have been deliberately set to be sub-optimal, 0.01 mC/cm at the threshold voltage for the high-V process, while the others are multiples of the typical electron exposure required to remove completely the H from the initial Si(001):H surface, and with gradually increasing voltage. Note that the top-right patch crosses a step edge to a higher terrace, so the direction of the dimer islands is reversed.

The first STM image already shows some difference between the patches. The overall size of the top-left patch is smaller than the other three, which results from a change in the linewidth of the electron beam. Furthermore, there are some black specks, which are either missing dimer defects or some remaining adsorbed H, in all four patches, but in the top-left patch, there is a larger black area in the lower center of the depassivated square (circled). After three cycles, most of a monolayer has been grown, and second layer islands have nucleated. However, there is a significant difference in the average size of the islands, and also in the overall disorder of the grown patches. In the three higher exposures, the islands are several dimer rows wide, and the first layer is nearly complete; the second-layer islands have even grown

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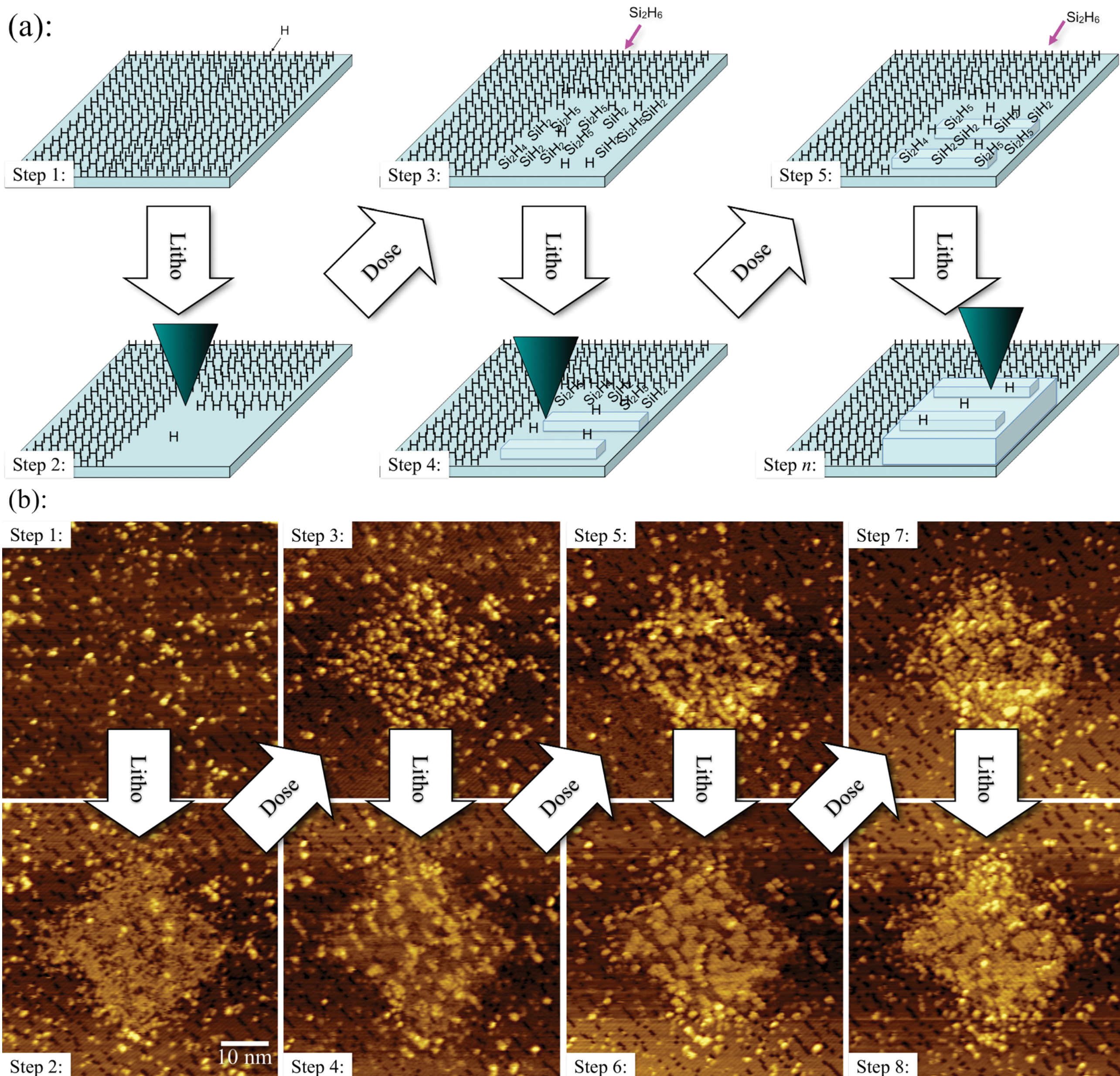

FIG 1. (Color online) (a): Schematic cartoon of the Patterned ALE process. Step 1: A H- terminated Si(001) surface is prepared, and stabilized at growth temperature; 550–600 K. Step 2: A pattern is created by STM lithography. Step 3: The tip is retracted, and disilane is dosed to saturated the pattern. Step 4: Repeat lithography to remove the H from the adsorbed disilane fragments. Step 5: Repeat the disilane dosing step. Step *n:* After many cycles of Steps 4 and 5, multiple monolayers of Si are built up. (b): Patterned ALE of Ge/Si(001) at 550 K. The sequence of pictures shows the same process as described schematically in panel (a). A pattern is created by STM lithography, using conditions, 9 V, 3 nA, and an electron exposure of 0.1 mC/cm. Three cycles of digermane dosing and lithography are used to grow a single monolayer island of Ge.

to widths of 2–3 dimer rows in some cases. For the lowest exposure, the first layer is much less complete, with a gap corresponding to the dark patch seen after the initial depassivation, the average island size is narrower, and the island shapes are rougher. After six cycles, close to 2 ML has been grown for the highest exposures, and third layer islands have nucleated. The first layer has therefore been completely filled in, and any gaps overgrown. The second layer islands are narrower than those on the first layer, but they are also filling in. Again, for the lowest exposure, the growth has been more disorderly. The first layer has never completely filled in, and the second layer islands have not reached the same coverage as for the other patches.

These qualitative observations can be reinforced by analysis of the coverage of each layer at each growth cycle, as shown in Fig. 2(b). The coverage of each layer has been extracted by leveling each island locally, and then thresholding the image so that the desired layer is white, and anything lower is black. The variability between analyses of the same island is a few percent of a ML. The amount of deposited Si is quite similar for the first few cycles, but while the first ML reaches a coverage close to 100% after four cycles for the three higher exposures, in the low-exposure case, the first ML never completely fills in. As a result, the coverage of the second ML does not rise as fast as for the higher exposures, and the third ML does not begin. The average growth rate in

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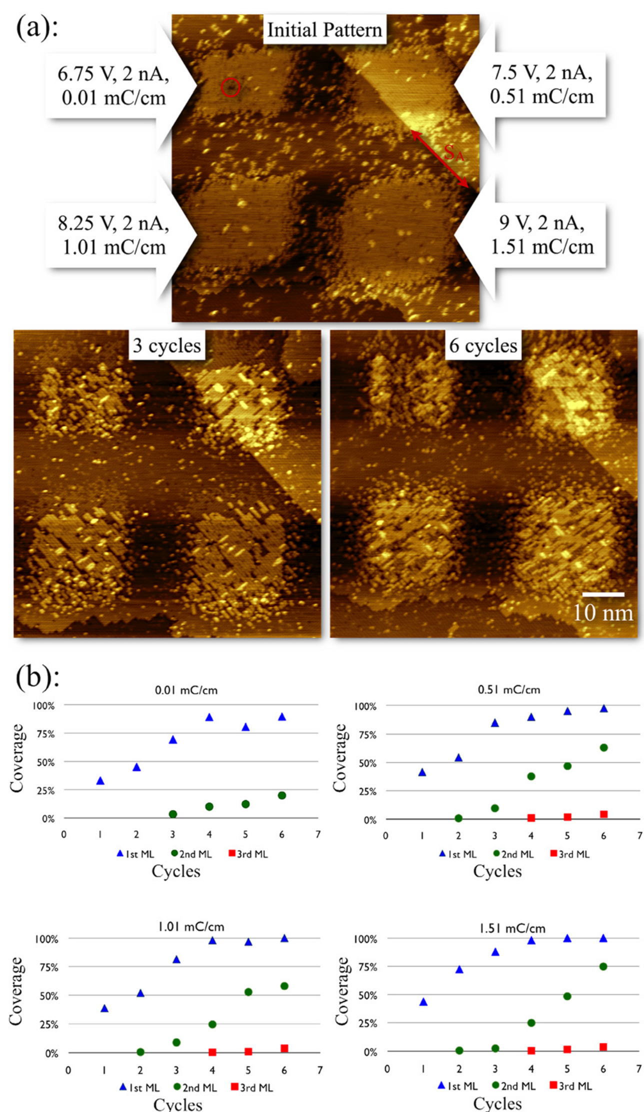

FIG 2. (Color online) (a): Patterned ALE of Si at 540 K. The 4 patches correspond to electron exposures of 0.01, 0.5, 1 and 1.5 mC/cm, from top-left to bottom-right. The three images are after the initial lithography step, after three cycles, and after six cycles of deposition and lithography. A dark area in the top-left patch is marked by a circle. A single A-type step is marked by the arrow as S_A. (b): Coverage analysis for the Si growth shown in panel (a). The first ML coverage is shown by the triangular symbols, the second ML by the circles, and the third ML by squares. For the lowest exposure growth, it is evident that the first ML never completely fills in, although the other patches have reached 100% coverage after four cycles. The difference in the growth of the second ML is more dramatic.

the first ML is around 0.30 ML/cycle for the three higher exposures, while it is only 0.24 ML/cycle for the lowest exposure. For the second ML, the rougher surface, and any remaining H, will reduce the number of adsorption sites for incoming disilane. Thus, the growth rate drops in all cases for the second ML. For the lowest exposure, this drops to 0.12 ML/cycle, while the highest exposure, at 0.28 ML/cycle, maintains a deposition rate close to the first layer. The growth rates of the other two exposures fall to 0.23 ML/cycle, reflecting the disorder of the first layer compared to the original flat surface. Further studies to a larger number of layers will be necessary to see if these differences in growth rates, and other minor differences between the 0.51 and 1.51 mC/cm cases, become significant over time.

One feature of all these growth patches; however, is the roughness around the edges of the patterns. This is due to the high-voltage lithography parameters used; the probability of H removal decays slowly across the surface, so that some dangling bonds are removed even outside the edges of the pattern. Single dangling bonds are not reactive to disilane, but wherever a cluster of more than one dangling bond has been created, some silicon will be deposited outside the edges. The second cause of pattern edge roughness is a small error in positioning of the lithography pattern from cycle to cycle. We are working on automated drift correction to reduce the positioning errors as much as possible. Atomically sharp pattern edges can be achieved using the low-V lithographic process described above. In the low-V regime, below about 7 V, multiple electrons are required to break a single Si-H bond. As a result, the depassivation efficiency drops off much faster with distance, and extraction of a single H atom, or a pair of H atoms from a single dimer, has been demonstrated. However, due to the much larger electron doses required for this process, it is much slower than for the high-V process, and it may also be more sensitive to the configuration of the Si-H bond on the surface. We have therefore conducted tests to compare growth for the low-V lithography and the high-V lithography. The STM data is shown in Fig. 3, and the coverage data is shown in Fig. 4. In Fig. 3(a), two patches can be seen. For the left patch low-V lithography (4.5 V, 6 nA, 16 mC/cm) was used, while for the right patch, high-V lithography was used (8 V, 6 nA, 1 mC/cm) Note that the written pattern is the same size in each case. The left patch corresponds much more closely to the written pattern size for the reasons mentioned above, and has much cleaner edges, although this is lost somewhat over time, due to alignment errors in subsequent cycles.

Growth of the first monolayer proceeds smoothly in both cases. The average island size is smaller for the low-V case, but after four cycles, a nearly complete layer has been formed in both cases, with islands merging, and only antiphase boundaries between the remaining islands, as seen from the triangular symbols in Fig. 4. Nucleation of the second layer starts one cycle earlier for the high-V lithography case, due to the large central island which has formed there. By the 4th cycle, these islands have already broadened beyond simple dimer islands. These islands continue to grow, across any gaps in the first layer, and by the 6th cycle, are large enough for third ML islands to nucleate. This indicates that there is no barrier to fill-in of the APBs in this regime. For the low-V lithography case, the second-layer islands do not broaden beyond 2 dimer rows, and are also very short. This is likely to be due both to H adsorbed at the active 'B' ends of the dimer islands, and also to blocking of growth across the APBs. While the third ML nucleates two cycles behind the high-V case, as seen in Fig. 4, the growth front has become visually disordered and rough. By comparison, the growth in the high-V lithography case is very well-ordered.

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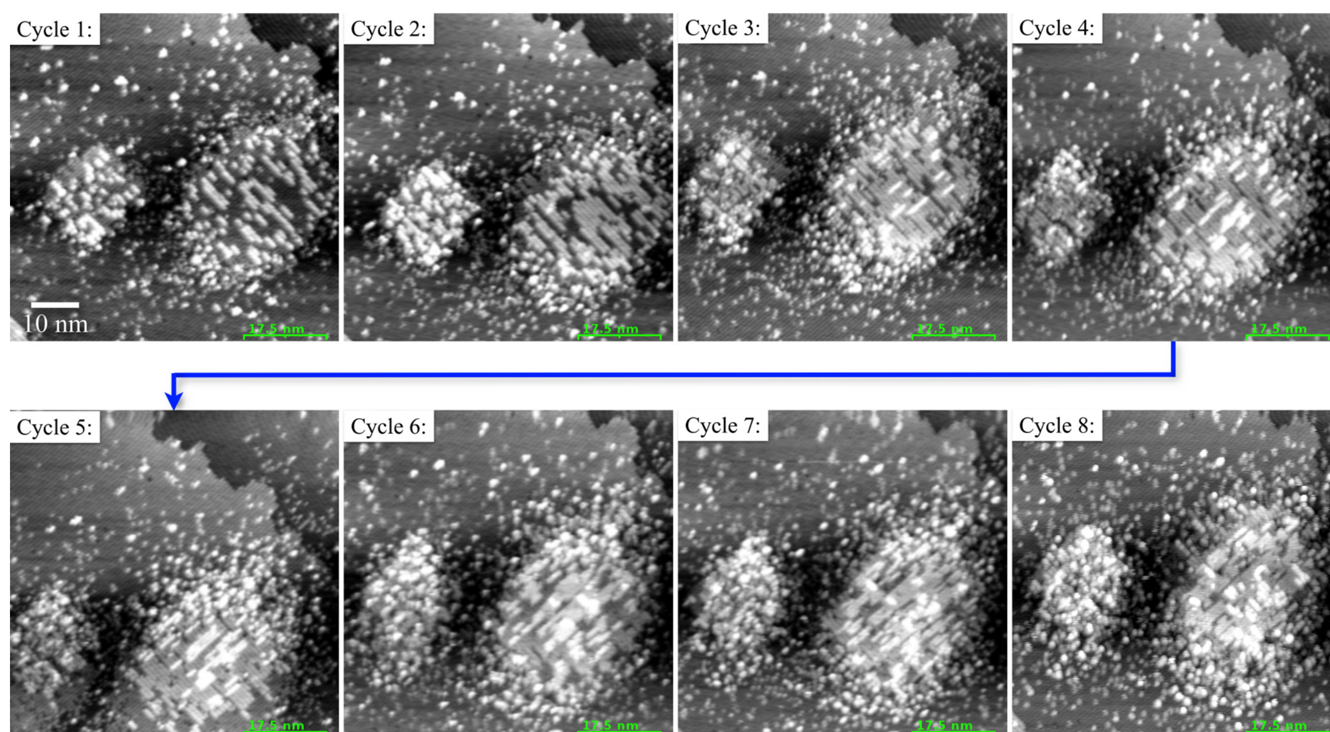

FIG 3. (Color online) Patterned ALE of Si at 540 K. The left patch is a low-V lithographic process, with conditions: 4.5 V, 6 nA, 16 mC/cm. The right patch is a high-V lithographic process, with conditions: 8 V, 6 nA, 1 mC/cm. Note that the written pattern is the same size in each case. The left patch corresponds much more closely to the written pattern size, and has much cleaner edges, although this is lost somewhat over time, due to alignment errors in subsequent cycles. The growth is quite similar in the first ML, but quite different in the second ML. The average island size is much smaller for the low-V case, than for the high-V case.

IV. DISCUSSION

The STM data shows that the growth of multiple layers of Si by the Patterned ALE process is feasible, but also that the quality of the grown layers is sensitive to the details of the depassivation process. The differences, both within different electron exposures for the high-V process, and also between the low and high-V lithographic cases, are much more dramatic in the second layer than in the first. Our interpretation of these data is that the growth quality depends upon the remaining H on the surface after depassivation. For the initial depassivation, all the H is in identical surface sites, as monohydride dimers, with one H bonded to each surface dimer atom. In this situation, the required electron dose to remove all the H is quite low. However, as shown in Fig. 5, on the growth surface there are a number of new sites available for adsorption. The steps parallel and perpendicular to the Si dimer rows are the A and B types respectively, following a convention by Chadi *et al.*[18] Where two islands meet, the dimerization of the top layer can be out of phase, and antiphase boundaries (APB) are formed. Again these can be parallel to the dimer rows (APB_A) or perpendicular to them (APB_B), as shown schematically in Fig. 5(a). The B-type APBs are a high energy site, and are the preferred nucleation site for new islands[17] as their local strain is relaxed when the dimerization is broken.[19] In Fig. 5(b), an example of this heterogeneous nucleation is marked. However, the A-type APBs are more important, as the growth direction of the second-layer dimer islands is perpendicular to them, as shown in Fig. 5(a). H adsorbed in the A-type APBs will prevent APB fill-in and therefore island growth.

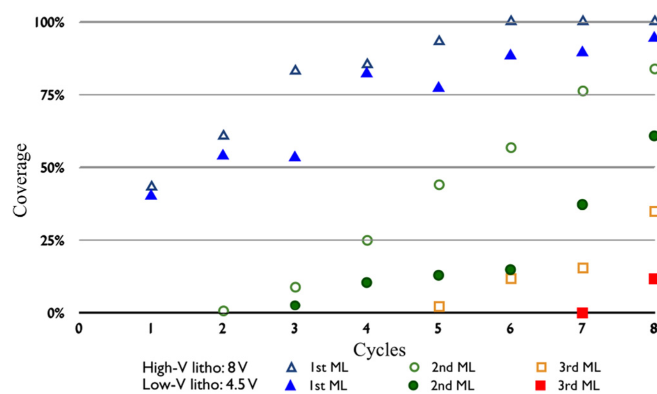

FIG 4. (Color online) Coverage analysis for the Si growth shown in Fig. 3 The first ML is quite similar in the two cases, but while the second and third layers nucleation and growth proceeds smoothly in the high-V case, for the low-V case, it nucleates later, and the total amount of Si deposited is much lower. N.B. The coverage of the second ML in the low-V case in cycles 7 and 8 are likely to be overestimations of the real coverage, as the many small islands add edge effects to the thresholding process used to analyze the data.

After deposition of disilane, the surface will be saturated by a variety of different Si- H configurations,[6,8] with surface SiH_2 and Si_2H_4 groups and monohydride ad-dimers. In each case, the yield of the depassivation process is likely to be different to the monohydride surface dimers. Previous work has found that while dihydride silicon loses H at a lower temperature in thermal desorption, the yield for electron-stimulated desorption is lower than for monohydride silicon.[20] Moreover, in some cases, the extra sites available on a rough growth surface, such as the ‘B’ sites at the ends of dimer

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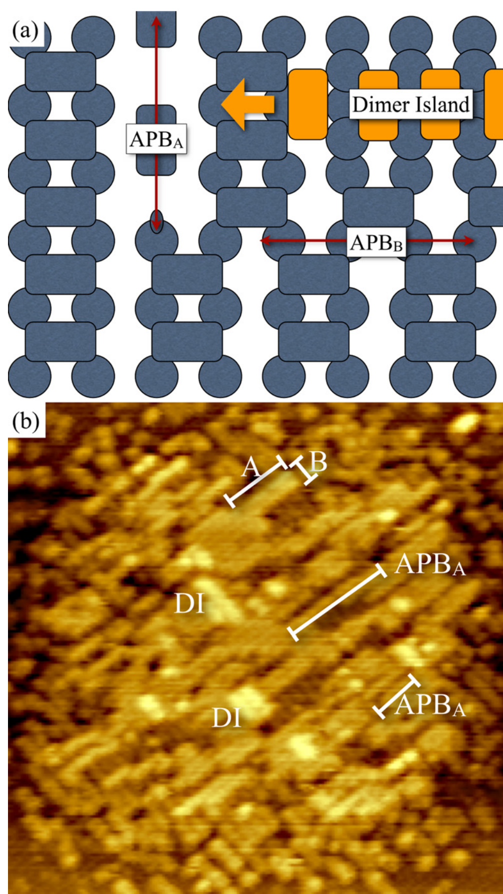

FIG 5. (Color online) (a): Schematic of a growth surface, showing the local structure of the two types of APBs. 'APB$_A$' and 'APB$_B$' refer to the A-type and B-type antiphase boundaries between islands. The APB$_B$ is characterized by a kink in the dimer rows, which causes local stress. A dimer island (DI) is also shown in yellow. Its growth direction, marked by the large arrow, crosses the APB$_A$, which therefore acts as a barrier to growth unless it can fill in. panel (b): STM image of a Si patch after several cycles of growth. Examples of the above features unique to the growth surface are marked. 'DI' mark second-layer islands. One has formed on top of a high-energy APB$_B$. 'A' and 'B' show the two types of step edges parallel and perpendicular to the dimer rows.

islands, provide more stable adsorption sites for H atoms than dimers on a flat surface, and thus any H adsorbed in these locations are likely to be more difficult to remove. For all these reasons, the average efficiency of the depassivation process will drop as growth proceeds, and it is necessary to increase the electron exposure to maintain complete depassivation. Secondly, the low-V lithographic process requires the injection of multiple electrons into a bond, in order to cause it to break. This process is likely to be much more sensitive to the local configuration of that Si-H bond; for example, whether it is dihydride versus monohydride. Thus the low-V process is likely to see a much more dramatic drop in depassivation yield on a growth surface than high-V lithography, as is seen in Fig. 3.

V. CONCLUSIONS

We have demonstrated Patterned Atomic Layer Epitaxy of Si and Ge at 550–600 K, to at least 2 ML. In the second and subsequent monolayers, the average island size and the deposited Si/cycle is dependent upon the electron exposure during the lithography step. Our explanation of this effect is that it is necessary to remove the last few percent of H atoms from the surface, which otherwise inhibit Si diffusion and island formation, In particular, in a growth context, adsorbed H atoms in special sites such as island ends and APBs block the overgrowth of gaps between first-layer islands, which severely limits the size of islands that form in the second and following layers. There are two lithographic processes: high-V lithography, above 7 V, is more efficient at removing H and achieving good-quality epitaxial growth, while low-V lithography allows removal of a single line of H atoms, giving pattern edges with atomic precision. Future work towards Atomically Precise Epitaxy is focusing on taller layers (~2 nm is now achievable, but is rough) and combining precise patterning, accurate alignment, and a smooth layer-by-layer growth process.

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